Gated Integrator for Point Detectors

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Introduction

Majority of experiments done by LCLS are pump-probe experiments that are used to study the ultrafast structural dynamics of atomic motions of matter in solid, liquid, and gas[1]. LCLS pump-probe experiments typically consist of optical pump, x-ray probe. An optical pulse is a pump beam that energizes a material into an excited state. An X-ray pulse is a probe beam used to measure the state of the material initiated by the laser excitation. LCLS uses a wide range of wavelengths for the pump-probe experiments. The time delays of the pulses range from a few femtoseconds up to 100 nanoseconds.

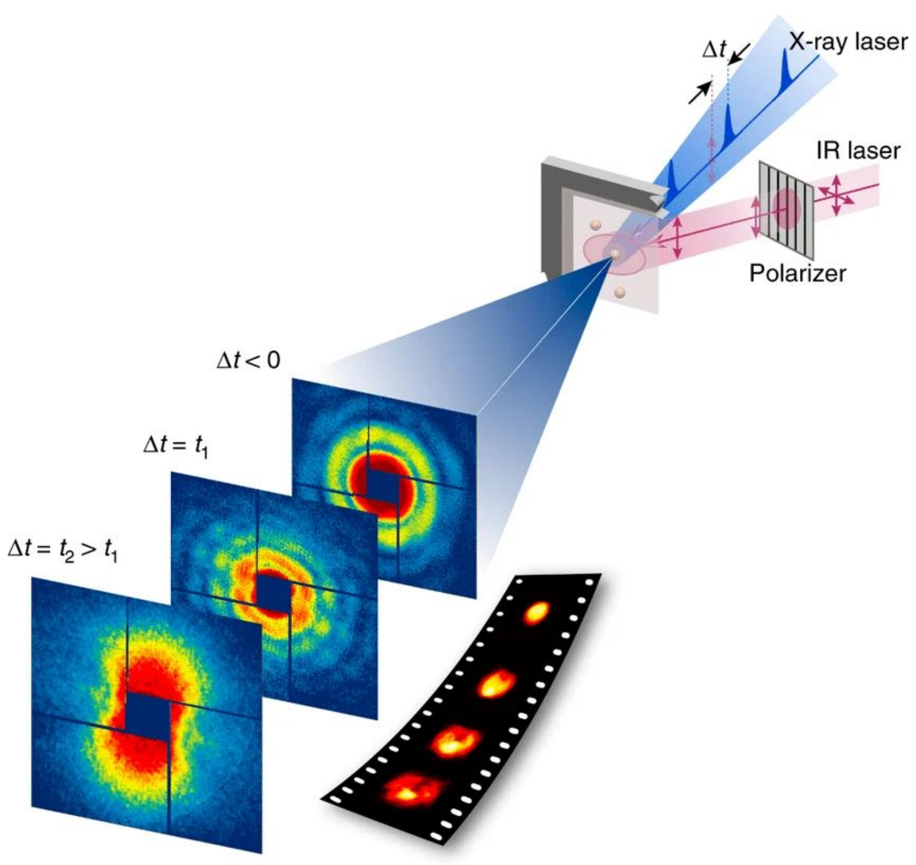


Fig. 1. Single-shot pump-probe imaging using femtosecond X-ray laser pulses[2]

Tabletop Integrated Laser Elements (TILEs)

LCLS developed a modular laser system called TILEs that provide many functionalities and components within a limited space. TILEs are installed in experimental hutches.

- **Functionalities:** Pulse compression, harmonics generation, beam steering, power control, and wavefront adjustment
- **Components:** Optics, motorized stages, beam diagnostics, and device controllers

To accommodate new features, custom printed circuit board (PCB) electronics are used to reduce footprint.

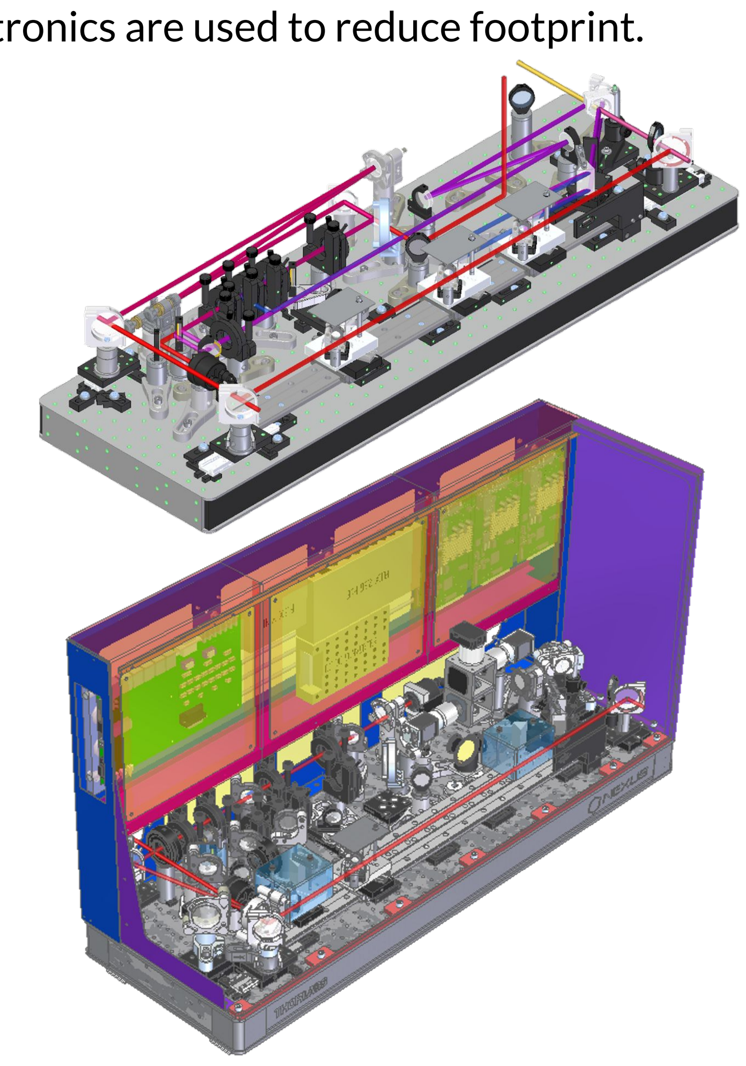


Fig. 2. TILEs with many components and functionalities

Gaussian Approximation of Laser Pulses

A Gaussian pulse is a signal defined by a bell-shaped curve:

$$f(t) = A_0 e^{-\frac{(t-t_0)^2}{2\sigma^2}} \quad (1)$$

where A_0 is the peak amplitude, t_0 is the center time of the peak pulse, and σ is the standard deviation parameter.

The laser pulses with wavelengths of either 800 nm or 1030 nm are modeled as a Gaussian pulse with a 20 ns full width at half maximum (FWHM) and approximately 1 V peak amplitude.

$$V(t) = V_0 e^{-4\ln(2)\left(\frac{t^2}{2\left(\frac{20\times10^{-9}}{2\sqrt{2\ln(2)}}\right)^2}\right)} \quad (2)$$

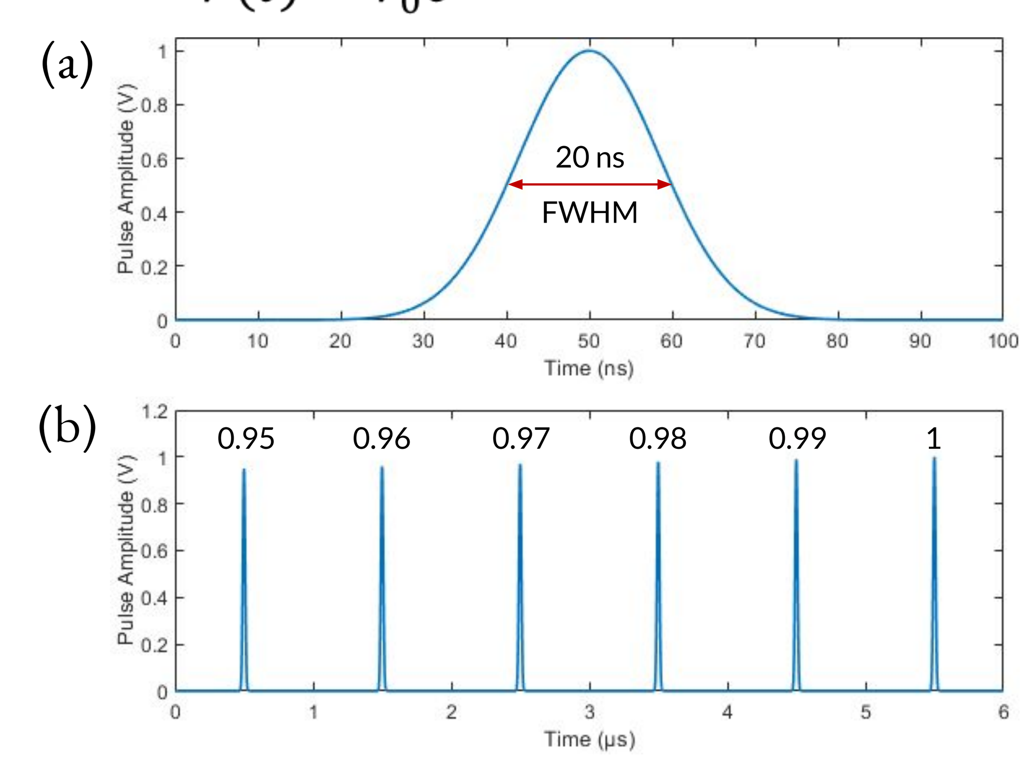
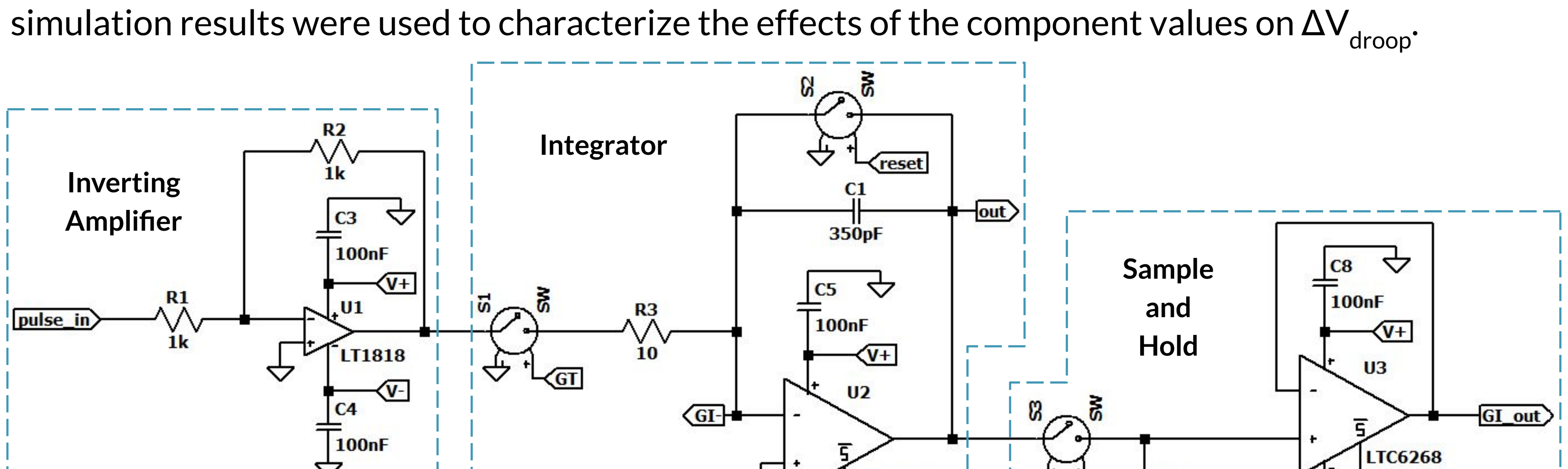
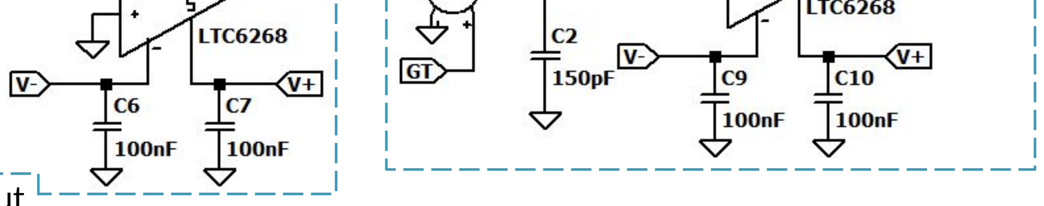


Fig. 3. **(a)** Gaussian pulse with 20 ns FWHM and 1 V peak amplitude. **(b)** Gaussian pulses with 20 ns FWHM, 1 µs period, and peak amplitudes increasing from 0.95 to 1 V.

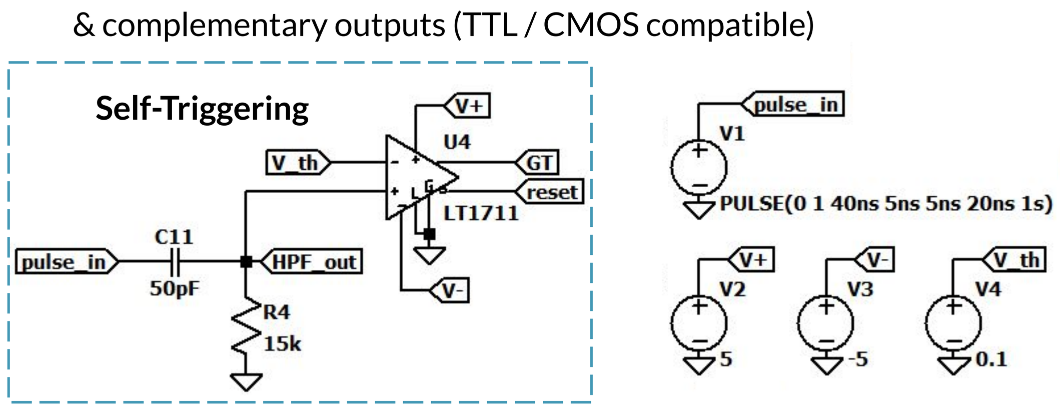
Gated Integrator Design

The gated integrator circuits were designed in LTspice to analyze the circuit behaviors and output voltage droop ΔV_{droop} from the simulations by sweeping the values of R_{in}, R_{fb}, C_{int}, and C_{hold}. The simulation results were used to characterize the effects of the component values on ΔV_{droop}.





- **LT1818:** 400 MHz BW, 2500 V/µs slew rate, 6 nV/√Hz noise and distortion
- **LT1711:** Ultrafast 4.5 ns comparator, rail-to-rail input & complementary outputs (TTL / CMOS compatible)
- **LTC6268:** 500 MHz FET-input, ±3 fA input bias current
- **TS12A4514:** SPST CMOS analog switch, 20 Ω R_{ON}, 1 nA leakage current, fast switching speeds (t_{ON} = 80 ns & t_{OFF} = 50 ns)




```
.tran 3s
.model SW SW(Ron=2 Roff=10e9 Vt=0.8)
```

Fig. 4. Gated integrator for point detectors schematic in LTspice. The signal from the laser pulse transducer (e.g., diode, power meter) is simulated using `PULSE(0 1 20ns 5ns 5ns 20ns 1s)`. The self-triggering circuit based on an RC edge detector generates the gate trigger and reset pulses. The gated integrator circuit will be connected to the laser pulse detector output.

Gated Integrator Simulation Results for Parameter Sweeps

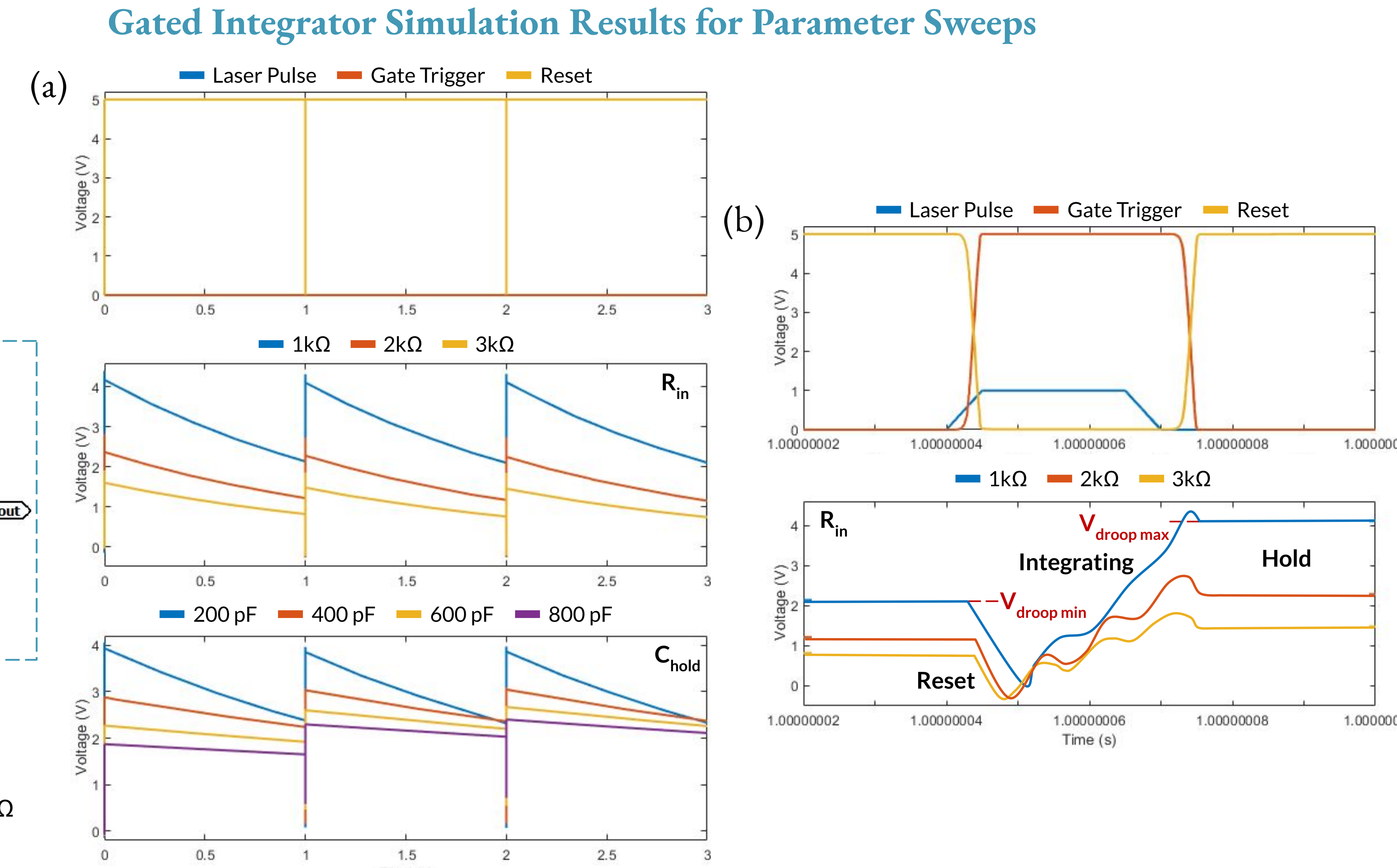


Fig. 5. **(a)** Simulated gated integrator pulses and output voltage $V_{GI\ out}$ of the circuit for parameter sweeps of R_{in} and C_{hold}. **(b)** Circuit behaviors and ΔV_{droop} during the integrating, hold, and reset modes for R_{in}.

Gated Integrator ΔV_{droop} for Parameter Sweeps

- R_{in} = 1kΩ / 3kΩ ΔV_{droop} ≈ 2 V / 705 mV
- R_{int} = 1kΩ / 3kΩ ΔV_{droop} ≈ 2 V / 1.9 V
- C_{int} = 200 nF / 800 nF ΔV_{droop} ≈ 2 V / 1.3 V
- C_{hold} = 200 nF / 800 nF ΔV_{droop} ≈ 1.5 V / 660 mV

Gated Integrator Operation Modes

- **Integrating:** Integrates the laser pulse
- **Hold:** Integration completes and holds the last integrated output voltage
- **Reset:** Resets the integrated output voltage to 0 V

Gated Integrator Design Requirements

- ≤5% output voltage droop within 1 second
- Small form factor (PCB, small connectors, repackageable)
- Accepts LVTTL triggers (0 to 3 V)
- Configurable gain and filtering

Future Work

- Generate a Gaussian pulse with 20 ns FWHM using a behavioral voltage source in LTspice
- Experiment the gated integrator circuit on breadboard in the lab and make adjustments to the circuit
- Design and fabricate a gated integrator PCB in KiCad

Acknowledgements

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