Developing and Validating a Hardware-in-the-Loop Continuous Integration Workflow for the LCLS-II Low-Level RF (LLRF) System

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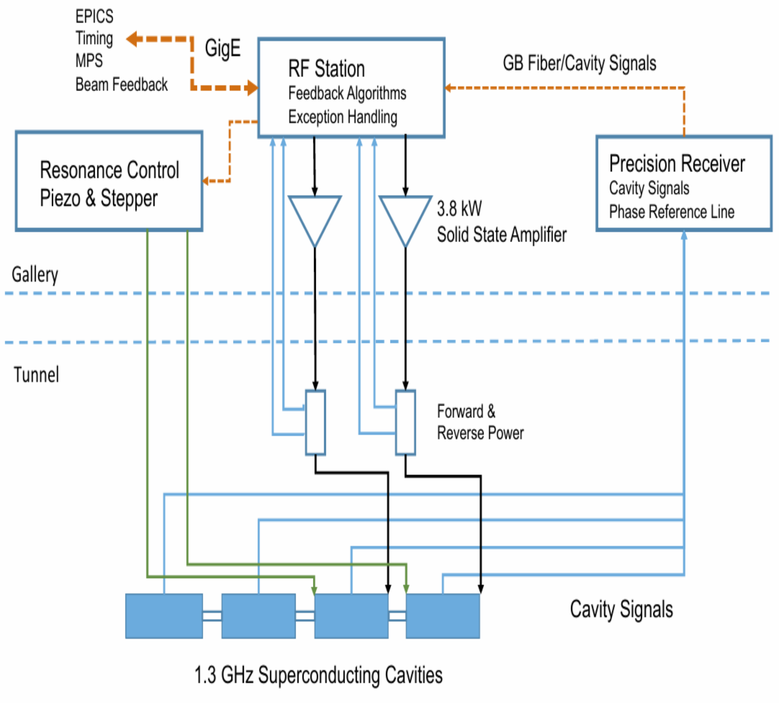
Linkedin

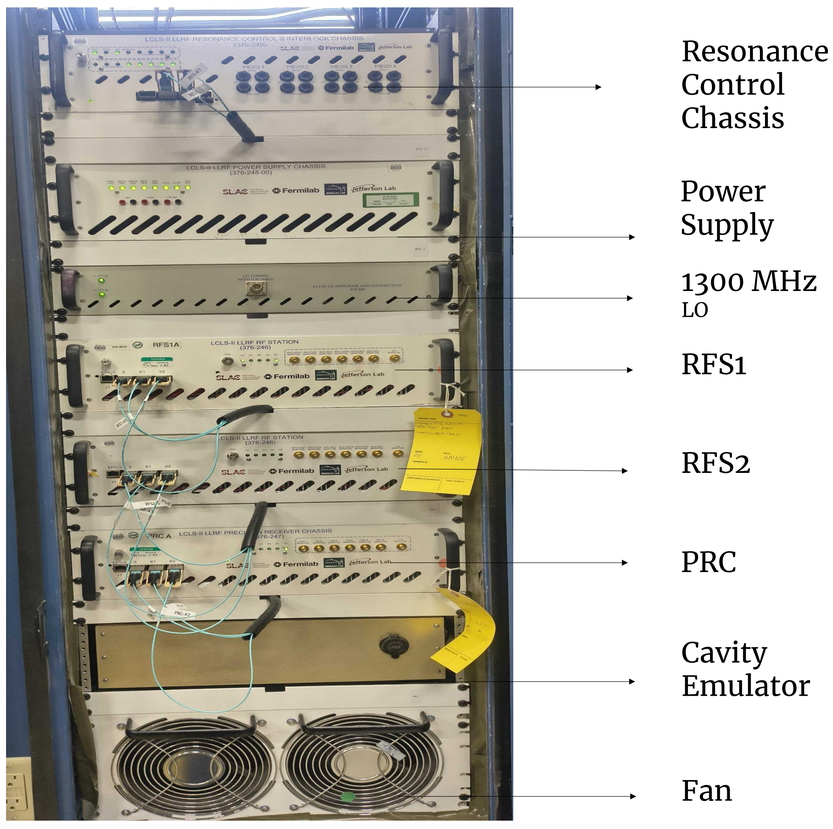
PRECISE RF CONTROL IS CRITICAL TO LCLS-II PERFORMANCE

Low-Level RF (LLRF) systems regulate the amplitude and phase of the RF fields that accelerate the LCLS-II electron beam. Meeting stability requirements as stringent as 0.01% in amplitude and 0.01° in phase requires reliable real-time digital control. FPGA firmware is therefore a critical part of accelerator operation and must be thoroughly validated before deployment.



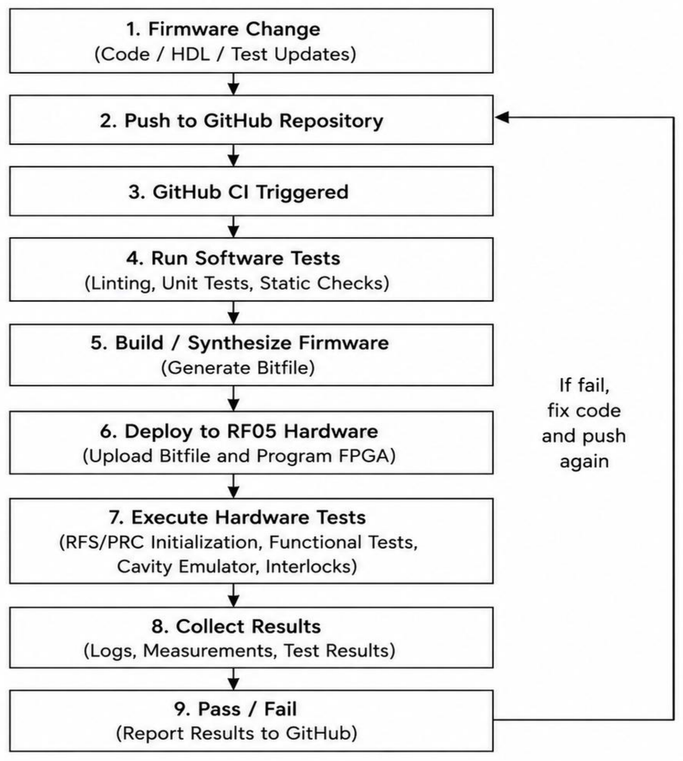
FIRMWARE IS VALIDATED ON PHYSICAL LLRF HARDWARE IN BUILDING 15

The RF05 test rack in B15 integrates two RF Station (RFS) chassis and a Precision Receiver Chassis (PRC) through dedicated optical links. The PRC downconverts the 1.3 GHz cavity signal to a 20 MHz IF, while the RFS chassis perform ADC/DAC processing, feedback, and self-excited-loop (SEL) control. FPGA firmware is exercised directly against this signal chain using a cavity emulator.



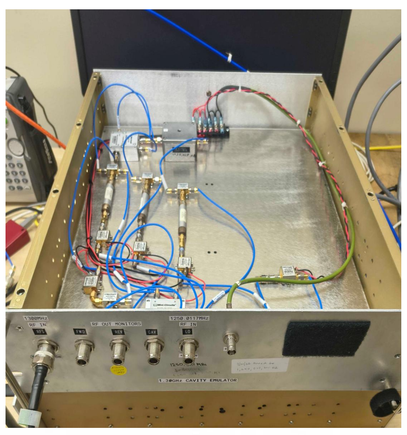
HARDWARE IN-THE-LOOP CI WORKFLOW

The CI sequence programs Kintex-7 FPGAs, verifies firmware identity through Git-ID readback, configures UDP/LEEP and optical inter-chassis communication, and executes rack-level hardware tests. Validation includes clock and ADC/DAC initialization, timing synchronization, CRC/link integrity, interlocks, SEL operation, and closed-loop RF control before returning pass/fail status.

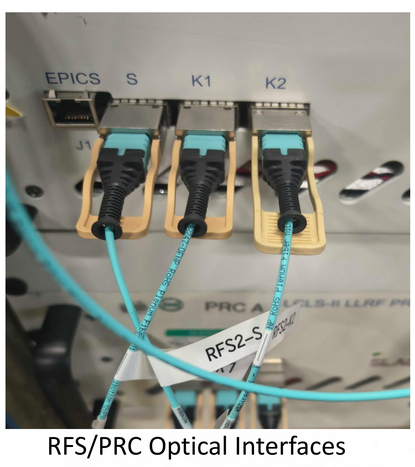


DEBUGGING SOFTWARE & HARDWARE VALIDATION

Manual execution of the CI test sequence exposed failures at multiple hardware interfaces. Each failure was reproduced and traced to its physical cause before the test sequence was re-executed, allowing validation to progress from FPGA programming through closed-loop RF control.

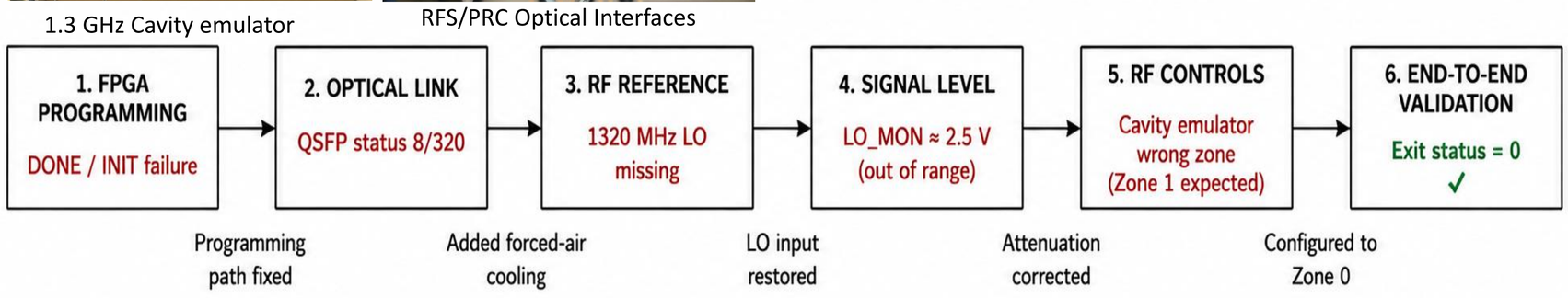


1.3 GHz Cavity emulator



RFS/PRC Optical Interfaces

- **Optical communication:** Recurrent QSFP Status 8/320 persisted after transceiver swaps and fiber replacement; forced-air cooling stabilized the links and restored normal Status 1.
- **RF reference chain:** Restored the required **1320 MHz LO** and corrected the LO monitor level from **~2.5 V to ~1.0 V** using attenuation.
- **Cavity-emulator configuration:** Matched rf_controls.py to the physical **Zone 0** connection, enabling the RF-control sequence to progress through pulse stretching and closed-loop CW operation.
- **End-to-end validation:** The complete manual lcls2_ci_SLAC.sh sequence reached controller zeroing and terminated with **exit status 0**.



RESULTS

Validation Stage	Test	Result
Kintex-7 FPGA Programming	Code / HDL / Test Updates	Pass
RFS / PRC Rack Checks	Hardware Sanity	Pass
Optical Communication (QSFP)	Link Status & CRC	Pass
Interlocks	All Interlock Conditions OK	Pass
Cavity Emulator / RF Controls	Zone 0 Configured	Pass
Closed-Loop Operation	SEL Running & Stable	Pass
Full Manual HIL Execution	Complete Test Sequence	Pass

Integrating physical LLRF hardware into CI enables SLAC to automatically validate firmware changes before deployment, reducing integration risk and improving the reliability of accelerator RF controls.

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[1] C. Serrano *et al.*, "Design and Implementation of the LLRF System for LCLS-II," *Proc. ICALEPCS 2017*, Barcelona, Spain, pp. 1969–1973, 2017.
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[3] T. O. Raubenheimer *et al.*, "The LCLS-II-HE, A High Energy Upgrade of the LCLS-II," accelerator-conference proceedings.